SESSION 7 – TAPA III
On-Die Power Supply Integrity

Thursday, June 17, 3:25 p.m.
Chairpersons: K. Bernstein, IBM
K. Seno, Sony

7.1 — 3:25 p.m.
Dynamic Power-Supply and Well Noise Measurement and Analysis for High Frequency Body-Biased Circuits, K. Shimazaki, M. Nagata*, T. Okumoto*, S. Hirano and H. Tsujikawa, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan, *Kobe University, Hyogo, Japan

Dynamic noises on power-supply as well as multiple wells necessary for body-biased circuits show frequency components strongly characterized by the interaction of circuit operation and AC transfer of biasing networks. Measurements with the resolution of 100-ps and 100-uV for a few 100-ns and 1-V ranges on multiple points in a product register file are performed at various operating frequencies up to 400 MHz and show the noises clearly emphasized infrequency domain by the interaction. A proposed analysis flow recruiting a fast SPICE simulator and parasitic extractors can predict the dynamic noises due to combined power supply, ground, well, and substrate interactions, and provide robustness to the design of body-bias control circuitry.

7.2 — 3:50 p.m.
A Built-In Technique for Probing Power-Supply Noise Distribution Within Large-Scale Digital Integrated Circuits, T. Okumoto, M. Nagata and K. Taki, Kobe University, Kobe, Japan

Noise detector circuits as compact as standard logic cells for being embedded within a high-density large-scale digital circuit enable in-depth characterization of dynamic power-supply and ground noises.Voltage drops at the locations of active cell rows within 1.8-V standard cell based digital circuits are consistently measured by 1.8-V and 2.5-V built-in detectors in a 0.18-um CMOS triple well technology. Measurements show that the ground-noise distribution is distinctively more localized than the power-supply counterpart due to the presence of a substrate.

7.3 — 4:15 p.m.
Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise, E. Alon, V. Stojanović and M. Horowitz, Stanford University, Stanford, CA

A technique for characterizing the cyclically time varying statistical properties and spectrum of power supply noise using only two on-chip samplers is presented. The samplers utilize a voltage-controlled oscillator to perform high-resolution analog-to-digital conversion with minimal hardware. The measurement system is implemented in a 0.13um process as part of a high-speed link transceiver. Measurement results showing the cyclo stationary behavior of power supply noise are presented.

7.4 — 4:40 p.m.
Power Supply di/dt Measurement Using On-chip di/dt Detector Circuit, T. Nakura, M. Ikeda and K. Asada, University of Tokyo, Tokyo, Japan

This paper demonstrates an on-chip di/dt detector circuit. The di/dt detector circuit consists of a spiral inductor under the power supply line which induces a di/dt proportional voltage, and an amplifier which amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement. The di/dt detector also measures the de-coupling capacitor effects for the di/dt reduction.

7.5 — 5:05 p.m.
Development and Validation of an Electromagnetic Distributed Power Grid Model for the 90nm Pentium® 4 Processor, T. Rahal-Arabi, G. Ji, M. Ma, A. Muhtaroglu and G. Taylor, Intel Corporation, Hillsboro, OR

In this paper, we show that it is necessary to include the distributed effects of the power grid to accurately model the power supply noise for high frequency microprocessors. We show that high frequency resonances can be entirely missed if such effects are not modeled. Finally we prove the theory with experimental validation on the 90 nm Pentium® 4 microprocessor.